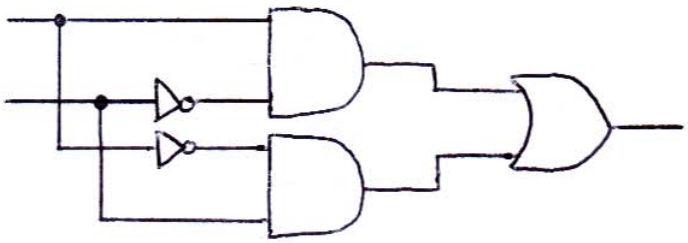
Lecture 25

XOR gate

A	B	X
0	0	
0	1	
1	0	
1	1	



Design procedure for combinational logic circuits

1) assign symbols

2) obtain boolean fcn
   a)
   b)
3) [optional]
4) draw the schematic

T	P	S	H
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

minterms –

maxterms –

output =

output =

Simplifying boolean expressions with Karnaugh maps ③

Consider 2-input fcn

A	B	minterm
0	0	
0	1	
1	0	
1	1	

$\bar{A}\cdot\bar{B}$	$\bar{A}\cdot B$
$A\cdot\bar{B}$	$A\cdot B$

$\bar{A}\cdot\bar{B}$	$\bar{A}\cdot B$
$A\cdot\bar{B}$	$A\cdot B$

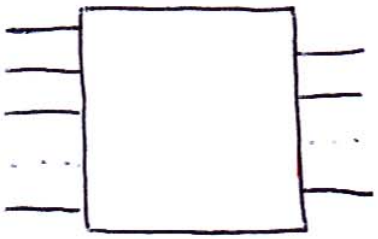
3-input fcn

4-input fcn

S \ TP	00	01	11	10
0				
1				

Programmable logic devices

- used to implement



- can generate

-

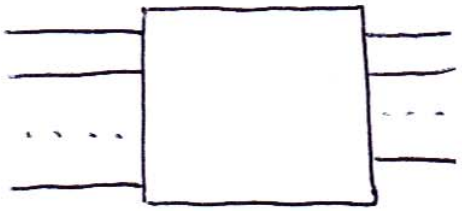
-

- some PLD types :

P3360/AEP3630

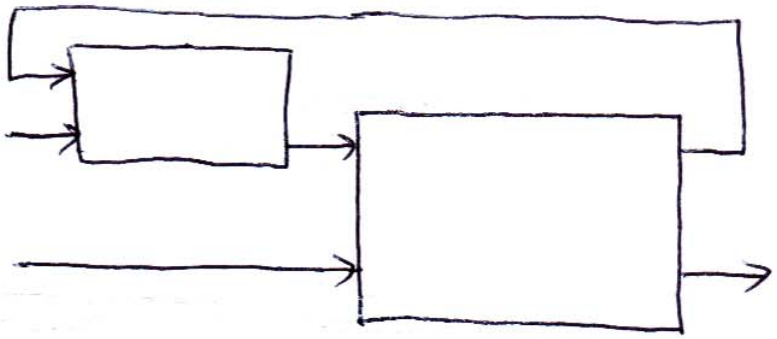
Lecture 27

Combinational Logic



- outputs depend _____ on present values of inputs

Sequential Circuit



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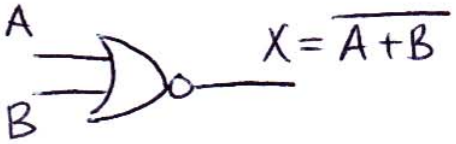
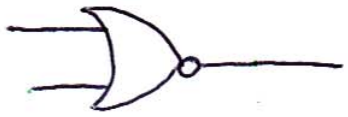
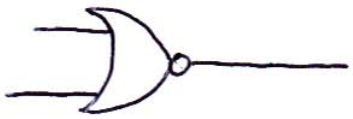
RS latch

recall NOR gate





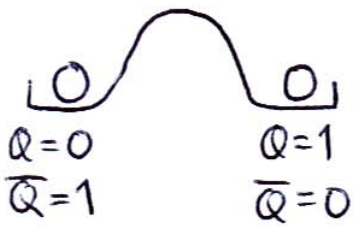


S	R	Q	$\overline{Q}$
0	0		
0	0		
0	1		
0	0		
1	0		
0	0		
1	1		
0	0		

S	R	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

– latch has _____ response,

– contrary to _____



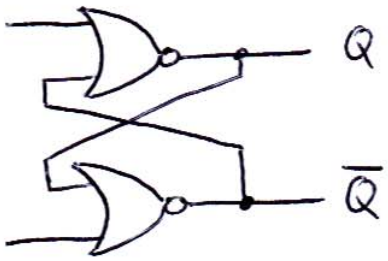
- similar to ball analogy, need a _____ to send the latch from one stable state into another
- there exists a min pulse length needed for switching

Flip-flop

problems with latches :

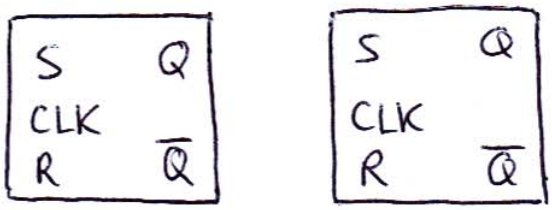
Improvements

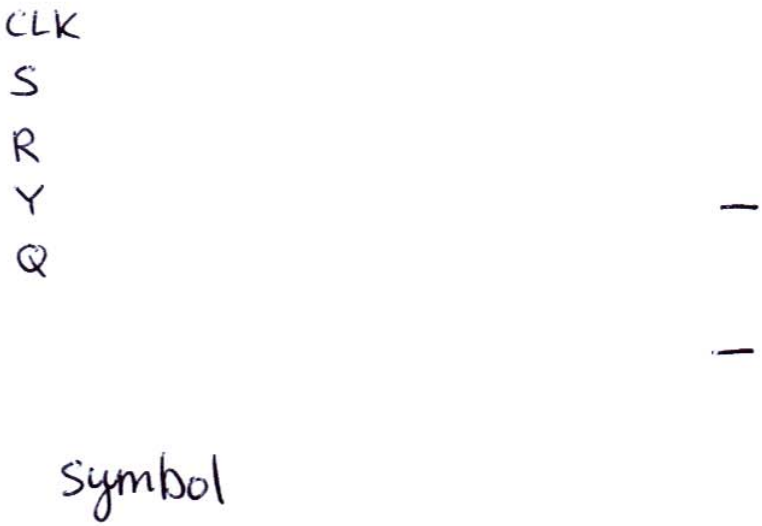
1) clocked RS flip-flop



2) triggering

Master-slave configuration





Symbol

3) direct inputs