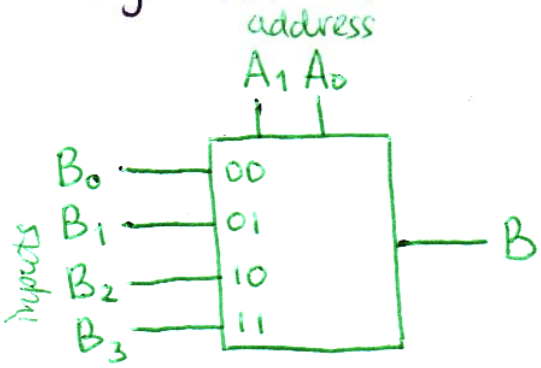
P3360 / AEP 3630

Lecture 28

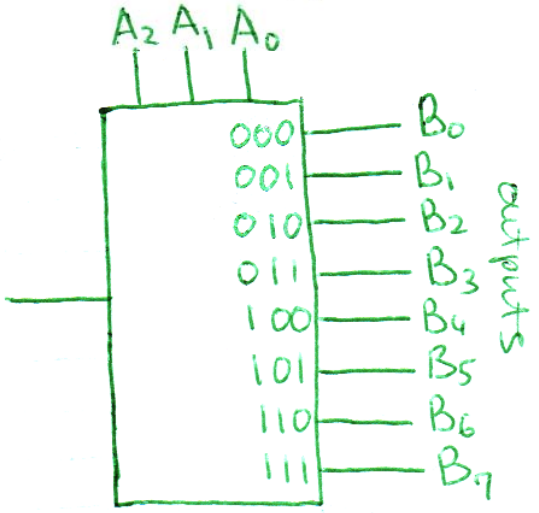
Multiplexer / Demultiplexer (mux/demux)

- combinational logic used to combine/distribute 2^n inputs/outputs addressed by n select lines into/from a single line

E.g. 4:1 MUX

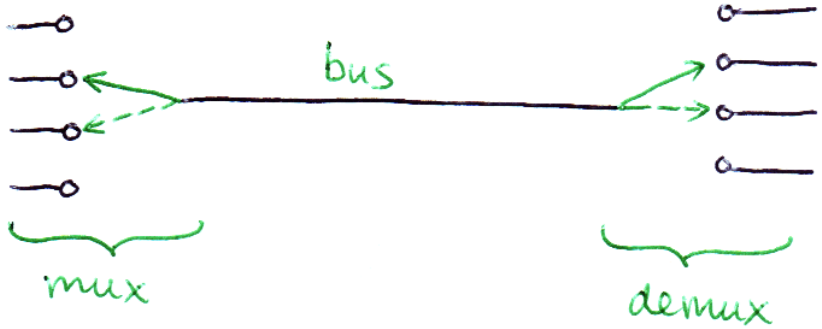


1:8 DEMUX



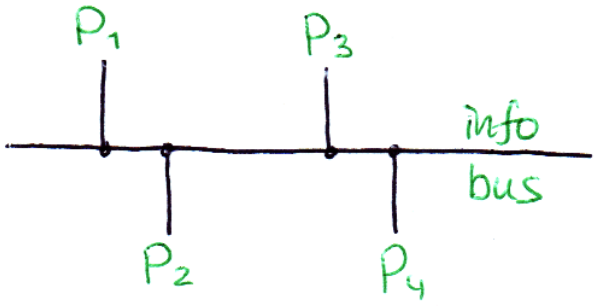
Applications

1) sharing bus (= data line)



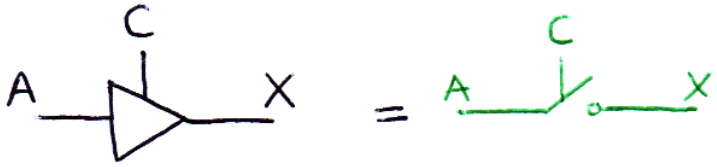
- Mux combines multiple inputs into a single data stream
  Demux splits the data stream into the orig. multiple signals

Also : can use 3-state logic



P_{1-4} – some peripheral logic devices

- cannot share usual 0/1 devices without confusion
- each device must have <u>tristate buffer</u>, which effectively removes all but one device from the bus



3-state buffer

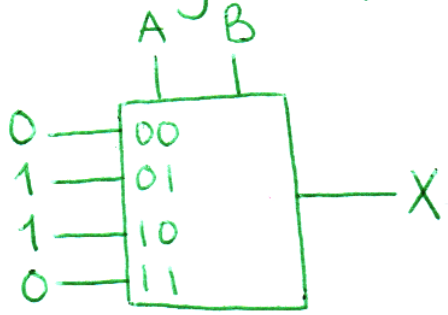
3 states:
- 0/1 logic
- Z high Z (open circuit)

2) Arbitrary logic implementation (cf. PLD)

$2^n:1$ mux can represent arbitrary n-input fcn

E.g. XOR

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0



3) Encoding / decoding (encoder/decoder – another name for mux/demux)

- turn one form of digital info representation into another / and back

BCD ↔ binary

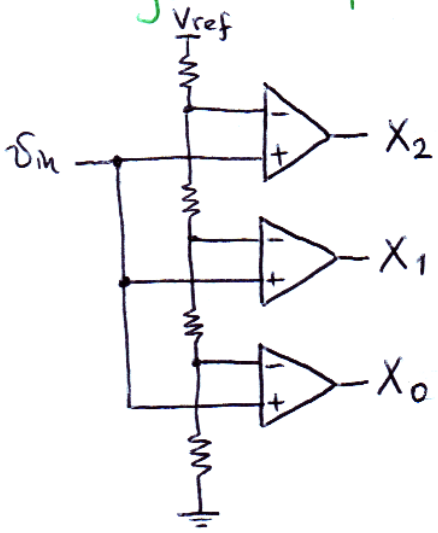
Gray ↔ decimal

.....

Example

Priority encoder

e.g. HW2 problem 3

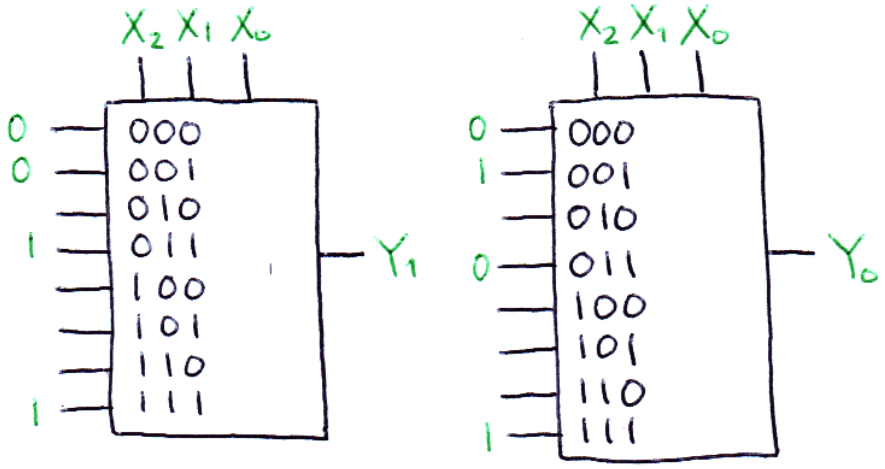


output from parallel ADC

$X_2X_1X_0$	Y_1Y_0
000	00
001	01
011	10
111	11

Need to convert to binary
(= priority encoder)

implementation
with two 8:1 muxes

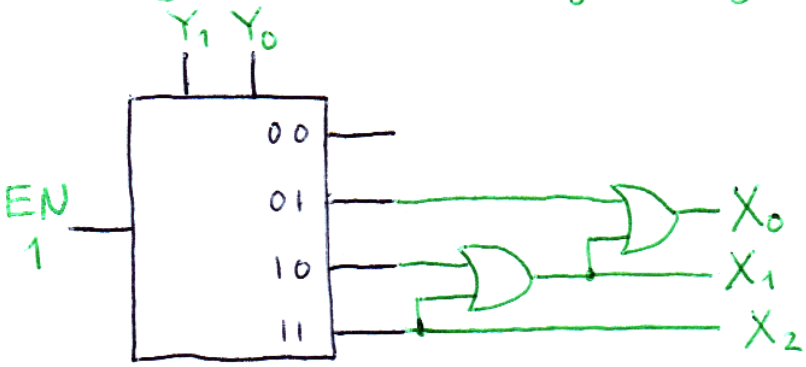


Priority decoder ?

E.g. strength bar display

LED

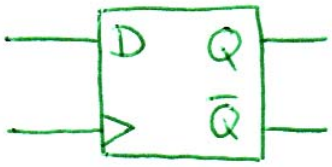
weak strong



Flip-flops (contd.)

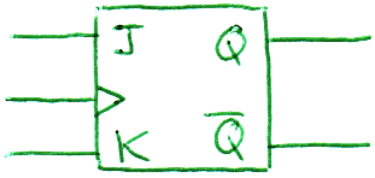
so far discussed RS flip-flop

D flip-flop (data - 1 bit memory)



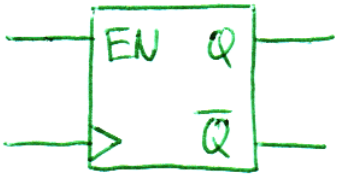
D	Q_{n+1} ← clock tick #
0	0
1	1

JK flip-flop



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

T flip-flop (toggle)



$Q_{n+1} = \overline{Q}_n$ when EN = 1

- any type of FF (+ combinational gates) can be converted into any other type

e.g. D → T