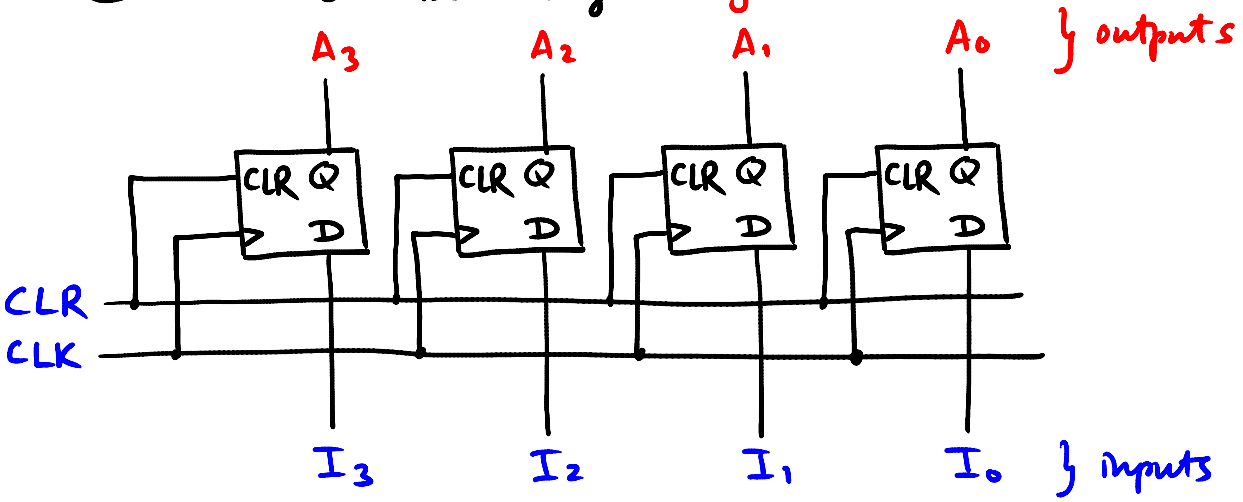
P3360/AEP3630
Lecture 29

FF aplications

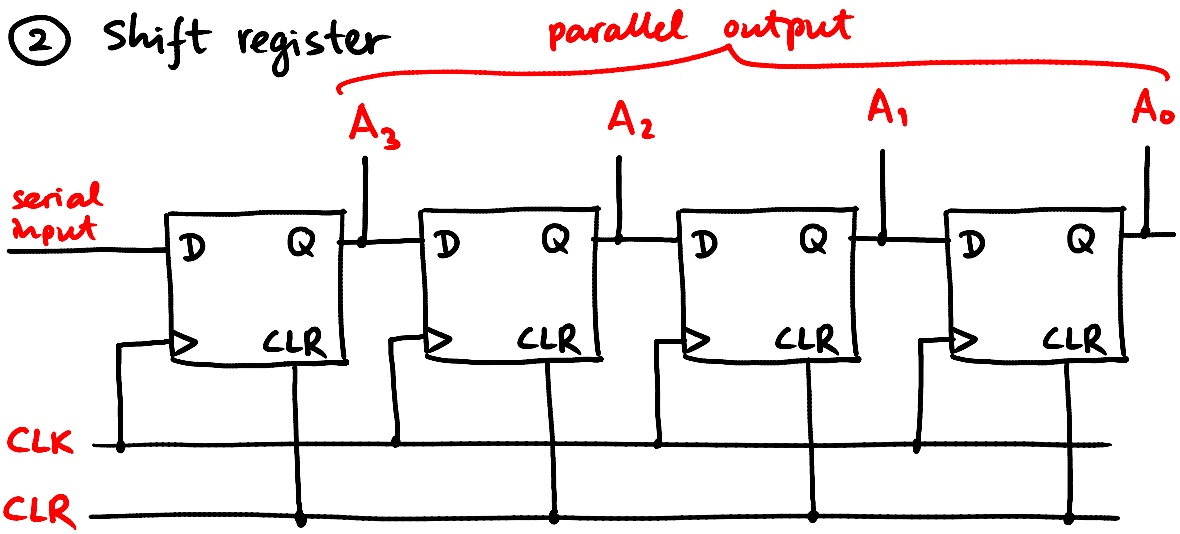
① Parallel data storage : register



* inputs (I_0-I_3) at ↓ edge of CLK are stored in the register

* CLR input clears the data asynchronously

② Shift register



* data shifts right after each CLK pulse

Apps :

* serial to parallel data conversion
  (transmit digit. info over serial connection)

* divide / multiply by 2
  (same as shift right / left)

* programmable delay

Timing terminology

transition time = time for FF output to go 0→1 or 1→0 after the input change (c.f. prop. delay)

setup time = min time inputs must be stable before clock pulse enables FF (~20ns)

hold time = min time inputs must be stable after the clock pulse enables FF (~100ps, essentially 0)

③ Counters, ripple counters (asynchronous)

T flip-flops ganged together

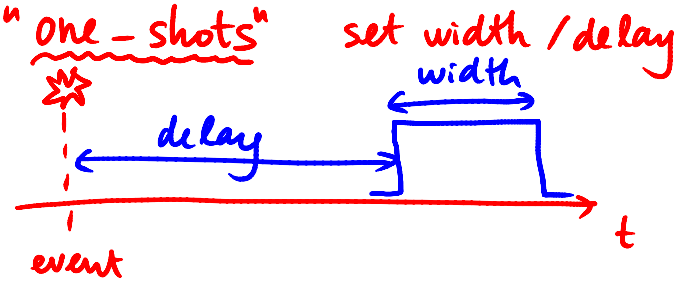
asynchronous vs. synchronous counters

"domino effect" : see LT spice ex.

0111 → 1000
actually can work as
0111 → 0110 → 0100 → 0000 → 1000
(glitch)

Timing circuits & clocks

* many cases when one needs to output a pulse at/after some event



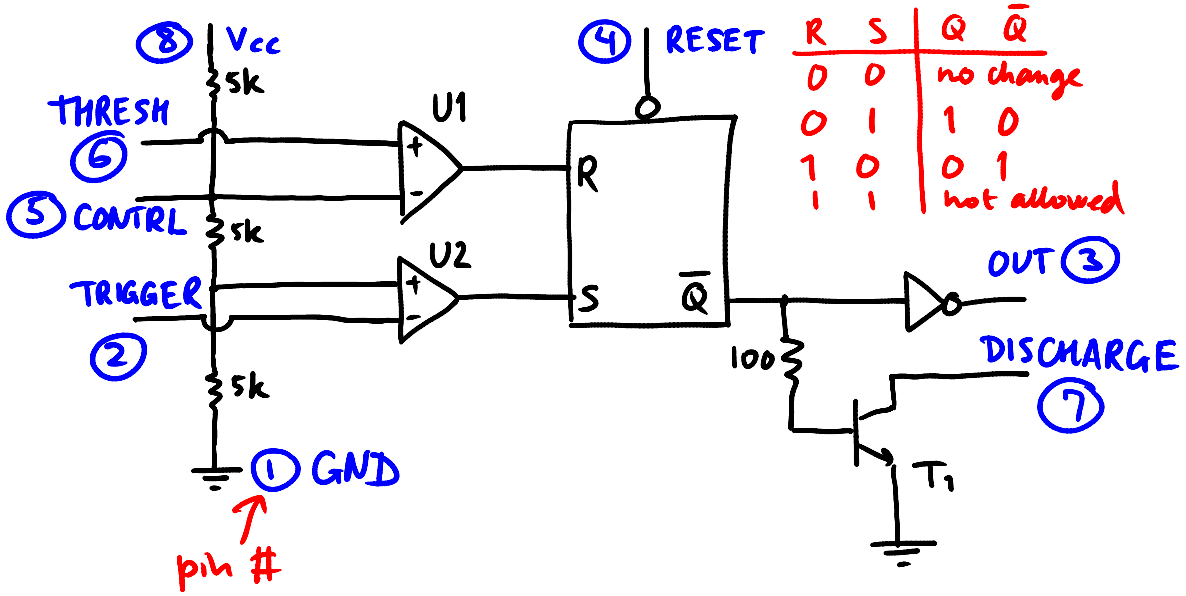
* clocks are important to synchronize sequential circuits

(need stable period, sharp rise/fall time)

Q: why need a precise clock?
A: E.g. watch "Longitude" (about John Harrison)

555 Timer

* 8 DIP package (like 741 op-amp)
* in part analog, in part digital
* can be wired as one-shot or as a clock (not very precise)



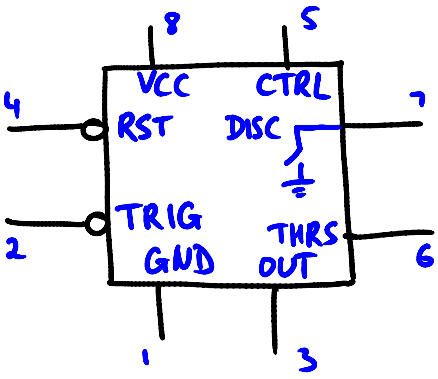
R	S	Q	Q̄
0	0	no change	
0	1	1	0
1	0	0	1
1	1	not allowed	

2 comparators $\frac{2}{3}V_{cc}$ & $\frac{1}{3}V_{cc}$ | RS latch | saturated switch

T_1 = ON if $\bar{Q} = 1$

T_1 = OFF if $\bar{Q} = 0$

Symplified symbol



supply voltage

$4.5V \leq V_{cc} \leq 16V$

output current

$(I_{out})_{max} \sim 200mA$

drives small loads all by itself

* as a one-shot : $T_w \sim 1\mu s \rightarrow 100s$

* as a clock : $f \sim 0.01Hz \rightarrow 1MHz$