Lecture 37

DAC specifications (same for ADC)

- bit resolution $= \frac{\Delta V_{max}}{2^n - 1}$ n = # of bits
- accuracy = deviation in the entire scale from specified value
- linearity = deviation of the output from best straight line fit
- setting time = time it takes for output to settle to within $\pm\frac{1}{2}$ LSB of the value

e.g. in the lab DAC 0808

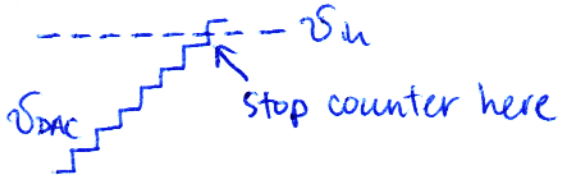
$n = 8$ bits

linearity $= \pm 0.2\%$

setting time $\simeq$ 150ns (~7MHz)

ADC (A/D converters) (see the printout)

staircase: value in counter after it is stopped $\propto v_{in}$ (uses D/A converter)



problems with staircase:

a) time to convert varies

$t_c \leq 2^n \underbrace{\Delta t}_{\text{clock tick}}$ (occasionally need to go thru full staircase)

b) susceptible to noise

not used in practice

successive approximation ADC

same as binary search algorithm

bits are set starting from MSB

1) begin by setting all bits to "0"
2) set MSB = 1 (DAC inside)
3) if $V_{DAC} < v_{in}$ leave MSB = 1
   otherwise MSB = 0
4) repeat 1-3 until all bits are set

Ex 3-bit ADC, 0-7V

$v_{in} = 2.5V$

DAC bits before	V_{DAC}		DAC bits after
100	4V	→	000
010	2V	→	010
011	3V	→	**010**

good: faster than staircase
fixed conversion time $n\Delta t$ (Δt: clock tick)

bad: still susceptible to noise

Flash ADC

- resistor ladder divides Vref into $2^n - 1$ identical segments
- input v_{in} simult. compared with each segment
- priority encoder provides binary output

good: fast (< 10ns conversion time)
bad: need $2^n - 1$ comparators (large #)

e.g. 8-bit = 255
12-bit = 4095

(typically limited to 8-bit ADC)

Integrating ADC
Dual slope ADC

- much better noise immunity
- built-in averaging

2 step process

1) a) counter is reset ; S_1 closed ; cap discharged

b) S_1 open ; S_2 connected to v_{in}

c) integrate v_{in} for $T_{fixed} = m\Delta t$ (clock tick)

$$v_1 = -\frac{1}{RC}\int v_{in}\,dt = -\frac{T_{fixed}}{RC}\langle v_{in}\rangle$$

(avg. over $m\Delta t$ time)

2) a) S_2 now connected to $-V_{ref}$, counter starts counting

b) when v_1 integrates back to 0, stop the clock

slope $\propto$ input voltage (v_{in} or $-V_{ref}$)

when will clock stop?

$$-\frac{m\Delta t}{RC}\langle v_{in}\rangle = \frac{\ell\,\Delta t}{RC}(-V_{ref})$$

(← step 2)

$$\langle v_{in}\rangle = \frac{\ell}{m}V_{ref}$$

(← step 1)

good: noise (spike in volt.) immunity (integrator)
accuracy indep. of R, C, Δt values
most commonly used (DVM - digital volt. meters)

bad: slow, conversion time $\sim (m+\ell)\Delta t$